CLAIMS

What is claimed is:

1. A signal power detector comprises:

an input coupling circuit operably coupled to receive a signal and to convert the signal into a first input and a rectifying input;

a rectifying operational amplifier including:

first input transistor operably coupled to receive the first input;

second input transistor;

rectifying transistor operably coupled to receive the rectifying input;

current source operably coupled to provide a reference current to the first input transistor, second input transistor, and the rectifying transistor;

first active input load transistor operably coupled to provide a first active load for the first input transistor and the rectifying transistor;

second active input load transistor operably coupled to provide a second active load for the second transistor;

active output load transistor operably coupled to mirror the reference current; and

output transconductance stage operably coupled to the active load transistor and to the first input transistor and the rectifying transistor, wherein the output transconductance stage provides a rectified output representing a peak value of the signal; and

a charge pump operably coupled to convert the rectified output into a corresponding current, wherein the corresponding current represents power of the signal.

2. The signal power detector of claim 1 further comprises a capacitor operably coupled to receive the corresponding current and provide a corresponding voltage that represents the power of the signal.

3. The signal power detector of claim 1 further comprises a feedback network operably coupled between the charge pump and the second input transistor.

4. The signal power detector of claim 1, wherein the signal is a single-ended signal and wherein the input coupling circuit further comprises:

filtering circuit operably coupled to filter the single-ended signal to produce a filtered single-ended signal, wherein the filtering circuit provides the filtered single-ended signal to the first input transistor as the first input, wherein the filtering circuit provides a DC ground as the rectifying input, and wherein the output transconductance stage provides a half wave rectified output representing the peak value of the signal.

5. The signal power detector of claim 4, wherein the filtering circuit further comprises:

first capacitor operably coupled to receive the single-ended signal;

resistor having a first node and a second node, wherein the first node of the resistor is coupled to the first capacitor and second node of the resistor is coupled to the DC ground; and

a second capacitor operably coupled to the first node of the resistor and to a DC ground, wherein the first and second capacitors scale the single-ended signal.

6. The signal power detector of claim 1. wherein the signal is a differential signal and wherein the input coupling circuit further comprises:

differential filtering circuit operably coupled to filter the differential signal to produce a filtered differential signal, wherein a positive leg of the filtered differential signal is provided as the first input and a negative leg of the filtered differential signal is provided as the rectifying input, wherein the output transconductance stage provides a full wave rectified output representing the peak value of the signal.

7. The signal power detector of claim 6. wherein the differential filtering circuit further comprises:

first input capacitor operably coupled to receive a positive leg of the differential signal;

second input capacitor operably coupled to receive a negative leg of the differential signal;

first resistor having a first node and a second node, wherein the first node of the first resistor is coupled to the first input capacitor;

second resistor having a first node and a second node, wherein the first node of the second resistor is coupled to the second capacitor, and wherein the second nodes of the first and second resistors are coupled to a common mode reference; and

common mode capacitor operably coupled to the first nodes of the first and second capacitors.

8. The signal power detector of claim 1 further comprises:

the first input transistor, the second input transistor. and the rectifying transistor are implemented as PMOS transistors; and

the first and second active input load transistors are implemented as NMOS transistors.

9. The signal power detector of claim 1 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as NMOS transistors; and

the first and second active input load transistors are implemented as PMOS transistors.

10. A radio frequency integrated circuit comprises:

a receiver section operably coupled to convert inbound radio frequency signals into inbound intermediate frequency signals;

transmitter section operably coupled to convert outbound intermediate frequency signals into outbound radio frequency signals; and

transmit/receive switch operably coupled to connect either the receiver section or the transmitter section to an antenna, wherein the transmitter section includes:

mixing module operably coupled to convert the outbound low intermediate frequency signal into a radio frequency signal;

power amplifier operably coupled to amplify the radio frequency signal to produce an amplified radio frequency signal;

bandpass filter operably coupled to filter the amplified radio frequency signal to produce the outbound radio frequency signal; and

transmit signal strength indication module operably coupled to monitor transmit power of the power amplifier, the bandpass filter, or the transmit/receive switch, wherein the transmit signal strength indication module includes:

an input coupling circuit operably coupled to receive the amplified radio frequency signal, the outbound radio frequency signal, or a transmit radio frequency signal as an input signal and to convert the input signal into a first input and a rectifying input;

a rectifying operational amplifier including:

first input transistor operably coupled to receive the first input;

second input transistor;

rectifying transistor operably coupled to receive the rectifying input;

current source operably coupled to provide a reference current to the first input transistor, second input transistor, and the rectifying transistor;

first active input load transistor operably coupled to provide a first active load for the first input transistor and the rectifying transistor;

second active input load transistor operably coupled to provide a second active load for the second transistor;

active output load transistor operably coupled to mirror the reference current; and

output transconductance stage operably coupled to the active load transistor and to the first input transistor and the rectifying transistor, wherein the output transconductance stage provides a rectified output representing a peak value of the signal; and

a charge pump operably coupled to convert the rectified output into a corresponding current, wherein the corresponding current represents power of the input signal.

11. The radio frequency integrated circuit of claim 10, wherein the transmit signal strength indication module further comprises a capacitor operably coupled to receive the

corresponding current and provide a corresponding voltage that represents the power of the signal.

12. The radio frequency integrated circuit of claim 10, wherein the transmit signal strength indication module further comprises a feedback network operably coupled between the charge pump and the second input transistor.

13. The radio frequency integrated circuit of claim 10, wherein the input signal is a single-ended signal and wherein the input coupling circuit further comprises:

filtering circuit operably coupled to filter the single-ended signal to produce a filtered single-ended signal, wherein the filtering circuit provides the filtered single-ended signal to the first input transistor as the first input, wherein the filtering circuit provides a DC ground as the rectifying input, and wherein the output transconductance stage provides a half wave rectified output representing the peak value of the input signal.

14. The radio frequency integrated circuit of claim 13, wherein the filtering circuit further comprises:

first capacitor operably coupled to receive the single-ended signal;

resistor having a first node and a second node, wherein the first node of the resistor is coupled to the first capacitor and second node of the resistor is coupled to the DC ground; and

a second capacitor operably coupled to the first node of the resistor and to a DC ground, wherein the first and second capacitors scale the single-ended signal.

15. The radio frequency integrated circuit of claim 10, wherein the input signal is a differential signal and wherein the input coupling circuit further comprises:

differential filtering circuit operably coupled to filter the differential signal to produce a filtered differential signal, wherein a positive leg of the filtered differential signal is provided as the first input and a negative leg of the filtered differential signal is provided as the rectifying input, wherein the output transconductance stage provides a full wave rectified output representing the peak value of the input signal.

16. The radio frequency integrated circuit of claim 15, wherein the differential filtering circuit further comprises:

first input capacitor operably coupled to receive a positive leg of the differential signal;

second input capacitor operably coupled to receive a negative leg of the differential signal;

first resistor having a first node and a second node, wherein the first node of the first resistor is coupled to the first input capacitor;

second resistor having a first node and a second node, wherein the first node of the second resistor is coupled to the second capacitor, and wherein the second nodes of the first and second resistors are coupled to a common mode reference; and

common mode capacitor operably coupled to the first nodes of the first and second capacitors.

17. The radio frequency integrated circuit of claim 10 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as PMOS transistors; and

the first and second active input load transistors are implemented as NMOS transistors.

18. The radio frequency integrated circuit of claim 10 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as NMOS transistors; and

the first and second active input load transistors are implemented as PMOS transistors.